## REMARKS

The above-referenced patent application has been reviewed in light of the Office Action, dated February 22nd, 2001, in which: Claims 5, 6 and 13-16 are rejected under 35 U.S.C. 112, second paragraph; claims 1-3, 5-7, and 11-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi (hereinafter "Takahashi(I)", US Patent No. 6,037,824); claims 10, 17, and 18-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi (hereinafter "Takahashi(II)", US Patent No. 5,982,689); claim 4 is rejected under 35 U.S.C 103(a) as being unpatentable over Takahashi(I). Reconsideration of the above-referenced patent application in view of the following remarks is respectfully requested.

Claims 1-24 are now pending the above-referenced patent application. Claims 1, 3, 10, 11 and 17 have been amended, and claim 2 has been cancelled. No new claims have been added.

The Examiner has rejected claims 5, 6 and 13-16 under 35 U.S.C. 112, second paragraph. The rejection of these claims by the Examiner is respectfully traversed.

According to the Examiner, "Regarding claim 5, the recitation ' a first and second inverter...and an inverted output terminal of said p-type sense amp.' On lines 2-6 is indefinite because it is misdescriptive. According to figure 5, the first inverter is (540, 550) and the second inverter is (560, 570)..." However, this is not what figure 5 shows. Quoting from the detailed description, page 10, lines 27-29, "The terminal of jam latch 590 being pulled up will be on a circuit path with a full gate delay, due to either inverter 520 or 530, plus a simple gate delay, due to either transistor 540 or 560." It is respectfully asserted that the Examiner has misinterpreted figure 5 and the associated detailed description, and claim 5 is, therefore, in condition for allowance. Claim 6 depends from claim 5, and it is respectfully asserted that claim 6 is, therefore, also in a condition for allowance.

Regarding claims 13-16, the Examiner has objected to the use of the word "comprising". It is respectfully asserted that the use of the word "comprising" in these claims is appropriate. It is well-established that the word "comprising" is an inclusive or open ended term. As stated in As stated in *Molecon Research v. CBS, Inc., 229 USPQ 805, 812 (Fed. Cir. 1986)*, "[t]he term 'comprising' denotes

a patent claim as being "open", meaning that the recitation of structure in the claim is open to additional structural elements not explicitly mentioned." It is respectfully asserted that the use of comprising in this context is permissible, and, therefore, claims 13-16 are in a condition for allowance.

The Examiner has rejected claims 1-3, 5-7, and 11-16 under 35 U.S.C. 102(e) as being anticipated by Takahashi(I). It is respectfully asserted that the foregoing claims, as amended, are in a condition for allowance.

It is well-established that in order to establish a *prima facie* case of anticipation under 102 of the patent statute, the Examiner must a provide prior art document that meets each and every element and limitation of the rejected claim. Therefore, even if a single element or limitation is not met by the asserted document, then the Examiner has not succeeded in establishing a *prima facie* case.

Applicants begin with claim 1. Claim 1 (as amended) recites:

" A circuit comprising:

a differential sense circuit;

a latch;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle, wherein said differential sense circuit is coupled to said latch in a push-pull configuration."

According to the Examiner, "Regarding claims 1 and 3, figure 3 of Takahashi shows a circuit comprising: a differential sense circuit (23); a latch (24); the differential sense circuit and the latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in the latch is retained for at least one clock cycle (clock CLK.)"

However, Takahashi(I) does not recite all of the elements of claim 1, as amended. As just an example, Takahashi(I) does not disclose a differential sense circuit coupled to a latch in a push-pull configuration. According to the Examiner, figure 7 of Takahashi(I) shows a differential sense circuit coupled to a latch in a push-pull configuration, however, figure 7 discloses a circuit that has a precharged configuration, and there is no push-pull effect disclosed. The push-pull configuration of the rejected claims and the precharged configuration disclosed by Takahashi(I) are materially different,

and, therefore, the rejected claims patentably distinguish from Takahashi(I). It is respectfully asserted that the cited patent clearly fails to meet each and every element and limitation of claim 1 as amended, and the allowance of claim 1 is respectfully requested.

Claims 3 and 5-7 depend upon and include all limitations of claim 1, and patentably distinguish from Takahashi(I) for at least the same reasons as claim 1, as amended. It is, therefore, respectfully asserted that claims 3 and 5-7 are in a condition for allowance.

Claim 11, as amended, patentably distinguishes from the cited patent for at least reasons similar to claim 1. It is, therefore, respectfully asserted that claim 11 is in a condition for allowance.

Claims 12-16 depend from and include all limitations of claim 11, as amended. It is respectfully asserted that claims 12-16 patentably distinguish from Takahashi(I) for at least the same reasons as claim 11, and are, therefore, in a condition for allowance.

The Examiner has rejected claims 10, 17, and 18-24 under 35 U.S.C. 102(e) as being anticipated by Takahashi(II). It is respectfully asserted that the foregoing claims, as amended, are in a condition for allowance.

Claim 10, as amended, depends from and includes all limitations of claim 1, as amended. It is respectfully asserted that claim 10 is patentably distinct from Takahashi(II) for at least similar reasons as claim 1, specifically that Takahashi(II) does not disclose a differential sense circuit coupled to a latch in a push-pull configuration. It is, therefore, respectfully asserted that claim 10 is in a condition for allowance.

According to the Examiner, "[F]igure 1 of Takahashi (689) shows an integrated circuit (IC) comprising: a plurality of datapaths at least one of said datapaths comprising: a differential circuit (not shown, with outputs D and DB) and a differential sense latch (CELL), wherein the differential sense latch comprises a differential sense circuit and a jam-latch coupled such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored in said jam-latch." It is respectfully asserted that the cited patent fails to meet all of the limitations of claim 17, as amended. As just an example, Takahashi(II) does not disclose a differential sense circuit coupled to a jam-latch in a push-pull configuration. It is respectfully asserted that the cited

patent clearly fails to meet each and every element and limitation of claim 17, as amended, and the allowance of claim 17 is respectfully requested.

Claims 18-20 depend from and include the limitations of claim 17. Therefore, these claims patentably distinguish from the cited patent for at least the same reasons as claim 17. It is respectfully asserted that these claims are in a condition for allowance.

The Examiner has rejected claim 4 under 35 U.S.C 103(a) as being unpatentable under Takahashi(I). The rejection of this claim by the Examiner is respectfully traversed.

According to the Examiner, "[F]igure 3 of Takahashi includes all the limitations of the present invention except for the limitation that the sense amplifier comprises a p-type sense amplifier. However, it is well known the art [sic] that the n-type or the p-type sense amplifier is used depending on the selection of supply voltages to make them conductive. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to use the p-type sense amplifier for the "low level" input signal." It is respectfully asserted that Takahashi(I) is lacking several of the elements of claim 4, and, additionally, Takahashi(I) does not even recognize the problem dealt with by the rejected claim. Therefore, it would not be obvious to one of ordinary skill how to modify Takahashi(I) in order to produce the subject matter of claim 4. It is, therefore, respectfully asserted that claim 4 is in a condition for allowance.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all claims, as amended, in this application are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-9427. Reconsideration of this patent application and early allowance of all the claims, as amended, is respectfully requested.

Respectfully submitted,

Howard A. Skaist

Howard A. Skaist
Senior Intellectual Property Attorney
Reg. No. 36,008

Dated: 6/15/01

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

*I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents, Washington, D.C. 20231 on:*

6·20·01
*Date of Deposit*

Angie Farr
*Name of Person Mailing Correspondence*

Angie Farr 6·20·01
*Signature* *Date*

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The following claims have been amended as follows:

1. (Amended) A circuit comprising:

a differential sense circuit;

a latch;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle, wherein said differential sense circuit is coupled to said latch in a push-pull configuration.

3. (Amended) The circuit of claim 1~~2~~, further comprising a sense amp, said sense amp and said differential sense latch coupled such that, in operation, differential signals present on differential output terminals of said sense amp cause an electronic signal to be stored in said differential sense latch.

10. (Amended) The circuit of claim 1~~2~~, further comprising a differential domino circuit, said differential domino circuit and said differential sense latch being coupled such that, in operation, differential output signals present on differential output terminals of said differential domino circuit cause a corresponding electronic signal to be stored in said differential sense latch.

11. (Amended) A method for storing electronic signals produced by a differential circuit comprising:

pre-charging said differential circuit;

evaluating said differential circuit;

sensing differential output signals via a differential sense circuit, wherein said differential sense circuit is coupled to a latch in a push-pull configuration; and

storing an electronic signal corresponding to said differential output signal.

17. (Amended) An integrated circuit comprising:

a plurality of datapaths, at least one of said datapaths comprising:

a differential circuit and a differential sense latch, wherein said differential sense latch comprises a differential sense circuit and a jam-latch coupled such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored in said jam-latch, wherein said differential sense circuit is coupled to said jam-latch in a push-pull configuration.